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Analogue to Digital Converter (ADC) – Bit Count superstition

Abstract
A common assumption is that the ADC bit count is the primary indictor of a digital measurement instrument's accuracy. That in turn leads to the belief that a greater number of bits would therefore result in a more accurate instrument. This document analyses the impact of bit count on typical electrical power measurements to demonstrate that quantisation error quickly becomes negligible when compared to overall system performance.

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Author	AAC
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1 INTRODUCTION

In the field of measurement instrumentation, where modern products convert analogue quantities into a digital readout, there is a common misunderstanding that accuracy is primarily dependent upon the number of bits in the ADC.

While the resolution of the ADC does contribute to the overall system performance, it is usually not the limiting factor in practical measurement and simply increasing the bit count will not yield greater system accuracy.

The true accuracy of a system is composed of the many stages of measurement, from the analogue signal conditioning, the conversion to a digital measurement and the mathematical post-processing carried out.

The continued shift towards purely digital systems leaves many engineers with little exposure to the analogue world and therefore they may not have an appreciation of the physical limitations that dictate the accuracy of their measurements.

In a purely analogue system with an analogue dial reading, the equivalent would be the belief that simply adding more graticules on the dial will produce a more accurate reading. From this example, we can easily recognise that beyond the ability to visually resolve the new scale, the actual accuracy of the system will continue to be dictated by the mechanical linkages moving the needles and the front end. The same is true of a modern digital system.

2 ADC OVERVIEW

Before considering an ADC in the application of power electronics, it is worth discussing some of the features of ADC that are often overlooked.

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2.1 BALANCE OF PERFORMANCE

As with most engineering decisions, the performance of an ADC involves the consideration of multiple features. Usually this is a balance of: resolution (bits), sample rate, bandwidth, linearity and cost.

The number of bits is often used as a headline figure for ADCs; it is easy to understand, and the subject of quantisation error is often taught to undergraduates. Yet, the true real-world performance of the device is far more complicated.

There are many different architectures but in general, the opportunity cost of increasing the number of bits involves a concession in some other performance characteristic of the device. In certain conditions, this can lead to a loss of bits.

2.1.1 Effective number of Bits (ENOB)

The ideal n-bit ADC would always provide n-bits of useable bits, but these devices are not ideal and the influence of many factors including linearity, noise and no missing code result in some bits being effectively unusable.

This is characterised as an effective number of bits and is contingent on the operation of the device.

These values are usually provided with ADC's and can be significantly lower than the headline spec for high frequency applications. The effectiveness of the ADC will also be impacted by the surrounding circuitry such as a poorly designed front end, injecting significant amounts of noise can further reduce this value.

3 BITS REQUIRED FOR RMS MEASUREMENTS

Given the need to balance the overall system performance and the knowledge that there is inevitably a law of diminishing returns, there remains the question of 'How many bits do I actually require?'.

The design considerations are very complicated but as an example, the RMS measurement of a sine wave is considered. This is the simplest waveform and is the foundation for AC power measurements.

$$v(t) = \sin(t)$$

This is a single sine wave with a true RMS value $\frac{1}{\sqrt{2}}$

The aim here is to demonstrate the impact of the quantisation error on measurements to illustrate why a point is reached, where an increase of bits has no benefit

3.1 SIMULATION SAMPLING AND QUANTISATION

To simulate the core function of an ADC, a continuous waveform of discrete samples will be taken and then quantised to the required resolution, then the RMS maths is performed.

In this example $10{,}000$ linearly spaced samples were taken then these values were rounded to the nearest quantised level.

The quantised steps were equally spaced between the max/min limits of the wave and the step size was given by:

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$$\Delta = \frac{Max(v) - Min(v)}{2^B - 1} \quad Where\ B\ is\ the\ bit\ count$$

The figure below shows the sine wave overlaid with the quantised waveforms from 6 bits to 18 bits.

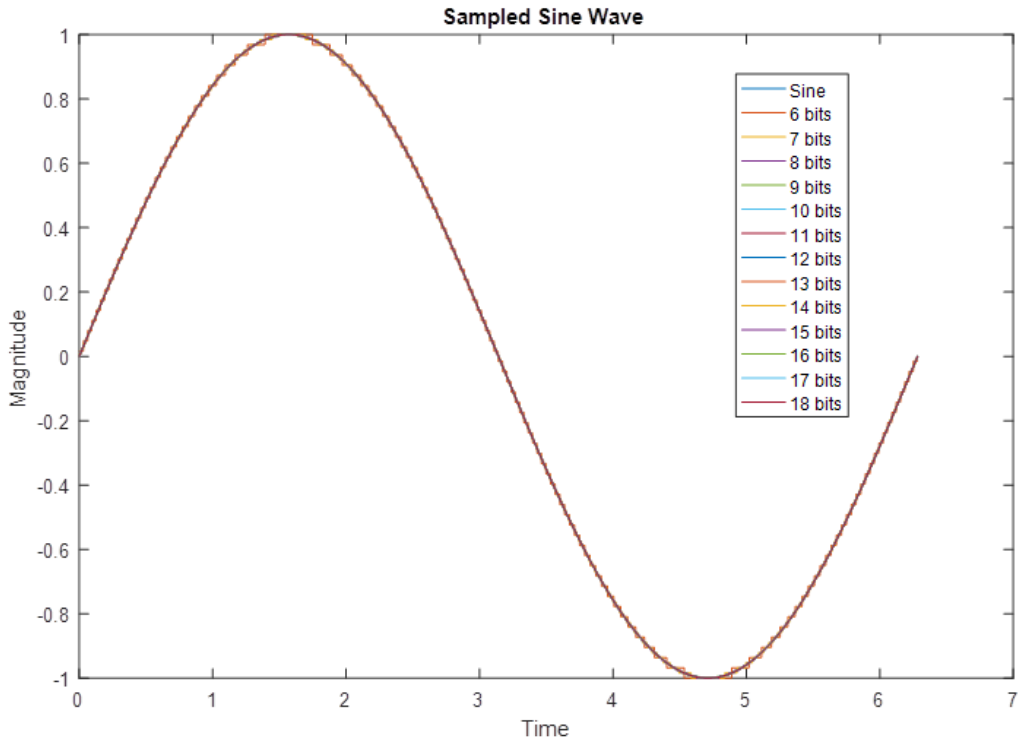

Figure 1: Quantised sine wave from 6 to 18 bit resolution.

3.2 RMS MEASUREMENT

The Root Mean Square (RMS) of the measurement was then taken for each of the digitised waveforms using the following discrete formula for RMS.

$$sampled\ RMS = \sqrt{\frac{1}{N}\sum_{n=1}^{N}(v(t_n))^2}$$

The error is then calculated by comparing to the true RMS of

$$error\ (\%) = \frac{sampled\ RMS - true\ RMS}{true\ RMS} \cdot 100$$

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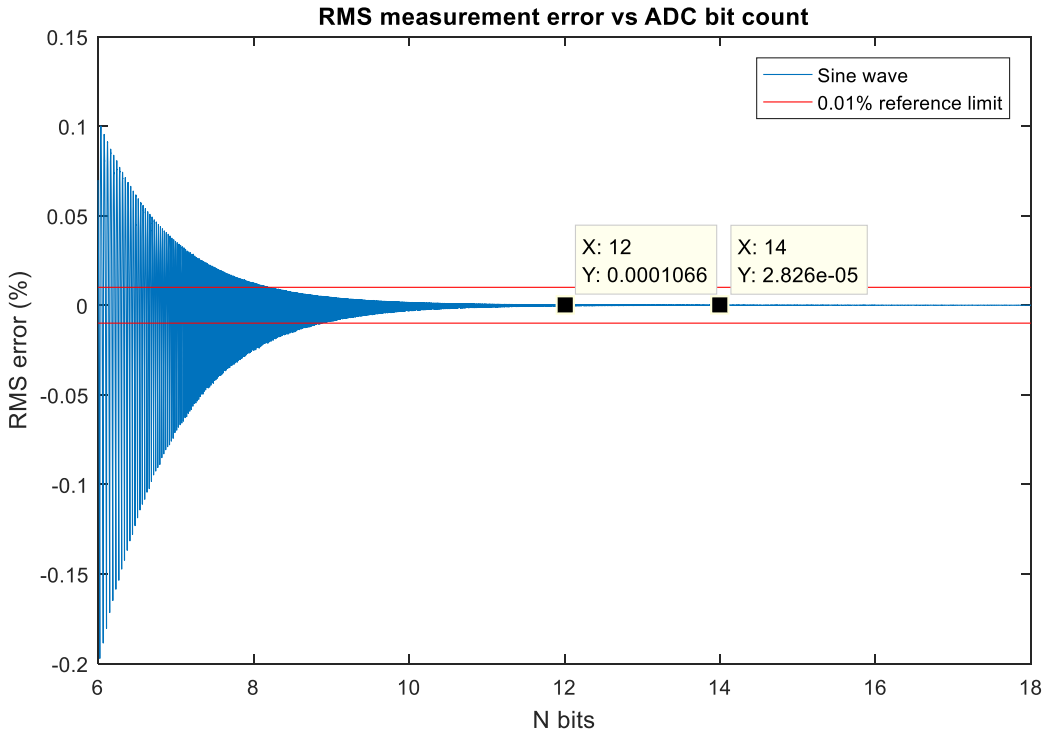

Figure 2: Sampled RMS error vs ADC bit count – 0.01% error shown for reference

Figure 2 shows the error from the number of bits[1] and a line in red which shows the typical specification for a high-performance power analyser at 0.01%. It is evident from this graph that the error contribution tends to zero but there are rapid diminishing returns. The contribution of error at even 10 bits is a small fraction of the defined accuracy, so it is therefore self-evident that the error is a small fraction of the total system error and, given this realisation, the route to high system performance is not to increase the number of bits.

How this relates to a more complex waveform is discussed in Section 3.6.

3.3 BUT WHAT ABOUT LOW RANGED SIGNALS

The example of RMS given in section 3.2 uses an ideally ranged signal. A reasonable counter to this result, is that the requirement from greater bit resolution remains to compensate for the effective loss of bits when a small signal, that only covers a fraction of the total measurement range, is applied.

3.3.1 Effective bit loss

In a fixed range system, this occurs when a signal is only using a fraction of the ADC range. If the signal is only half of the ADC's range, effectively a bit is lost, and so on as shown in the table below.

[1] As a DFT has been used, a non-integer number of bits has been simulated to ensure that the envelope of error is captured.

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Table 1: Effective bit loss	
Percentage of Range	**Bit loss**
50	1
25	2
12.5	3
6.25	4
3.125	5
1.5625	6
0.78125	7

It is clear to see that a signal at less than 1% of full range, will effectively lose 6 bits of resolution. This is very important on single range DAQ as they typically have a basic front end with a single, fixed range. For this reason, single DAQ's or basic measurement systems often attempt to continue to read small measurement using more bits.

In contrast to this, precision measurement instruments achieve low signal level analysis by ranging, which means that for most measurements, the waveform will always be greater than ~30% of range.

3.3.2 Hardware ranging and signal condition

An alternative approach to optimise the measurement signal is therefore through hardware ranging and coupling, so that measurement from the sensors (usually attenuators and shunts in power applications) utilise a greater proportion of the ADC input to maintain resolution.

For example, in a PPA55 the internal current ranges (peak) are $30mA$ to $300A$[2].

Taking the top range and a 14 bit resolution, the smallest step size would be:

$$\Delta = \frac{300 - (-300)}{2^{14} - 1} = 36mA$$

And the step size for the bottom range:

$$\Delta = \frac{30 \times 10^{-3} - (-30 \times 10^{-3})}{2^{14} - 1} = 3.66\mu A$$

Now, if this were a fixed range of 300A it would in theory require

$$required\ Bits = \log_2\left(\frac{300 - (-300)}{3.66\mu A} + 1\right) = 27.3$$

So, in theory, even if we ignore the impact of noise, a fixed ranged system would require **27 bits**, to achieve the same performance and dynamic range.

This ranging technique overcomes the need for a greater number of bits and ensures that the ADC is operating in the centre of its range. Good ranging techniques also have the benefit of

[2] Ranges and symmetric. -300 to +300A, and therefore the actual range is double the peak value.

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increasing the signal to noise ratio of the signal being analysed, so measurements are less influenced by other sources of error, such as noise that can dominate measurements.

3.4 WHAT ABOUT SMALL SUPERIMPOSED SIGNALS

A secondary question is 'what about small signals superimposed upon a large signal?'. The issue here being that there are often small components that need to be measured upon a large signal; these do not benefit to the same extent from hardware ranging since the range will be selected upon the peaks of the large waveform, and the small component may need represent a smaller fraction of the range.

In the power electronics field, a common example of these complex waveforms is the analysis of harmonics or a small signal with a large DC offset.

The DC offset is a simpler case, AC coupling can be used to isolate the AC components from the large DC and ensure that ranging is appropriate.

Analysis of harmonics is a more involved application and requires the use of a Fourier Transform to extract the harmonic components which are impacted less by the bit count.

An example is given in the following subsections.

3.4.1 An International Electrotechnical Commission (IEC) standard

Selecting a waveform for demonstration is not too easy, because the waveforms can vary significantly between applications.

However, one stringent application for harmonics is the IEC 61000-3-2 Electromagnetic Compatibility (EMC) standard which limits the harmonic current emissions.

For this example, we use the Class D harmonic limits where the dynamic range of harmonic measurements are most demanding.

3.4.2 The waveform

A waveform with a high crest factor is challenging since the range of the instrument will have to be increased to capture the peak. This means that the small harmonic components will therefore represent a smaller percental of range and therefore have the fewest number of effective bits.

To create the wave, the harmonics limits were calculated using the limits defined in the standard, with an assumed 600 watts in the fundamental.

The phase angle of the alternate odd harmonics (3rd, 7th, 11th etc) was set to 180 degrees so that they constructively interfere to produce a "peaky" (high crest factor) waveform; this makes the waveform more challenging as it maximises the dynamic range between the harmonic magnitude and total peak.

Table 2: IEC example waveform - harmonics

Harmonics	RMS (A)	Mag (A)	Phase (Deg)
1	2.6087	3.6893	0
3	1.4425	2.0400	-180
5	0.8061	1.1400	0
7	0.4243	0.6000	-180

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Table 2: IEC example waveform - harmonics			
Harmonics	**RMS (A)**	**Mag (A)**	**Phase (Deg)**
9	0.2121	0.3000	0
11	0.1485	0.2100	-180
13	0.1256	0.1777	0
15	0.1089	0.1540	-180
17	0.0961	0.1359	0
19	0.0860	0.1216	-180
21	0.0778	0.1100	0
23	0.0710	0.1004	-180
25	0.0653	0.0924	0
27	0.0605	0.0856	-180
29	0.0563	0.0797	0
31	0.0527	0.0745	-180
33	0.0495	0.0700	0
35	0.0467	0.0660	-180
37	0.0441	0.0624	0
39	0.0419	0.0592	-180

Using the harmonics in **Table 2**, the waveform can be constructed in the time domain, Figure 3. This has also been overlaid with a 12-bit quantised waveform. This is not readily visible at this zoom level, so Figure 4 shows a magnified version with a step size of ~4mA.

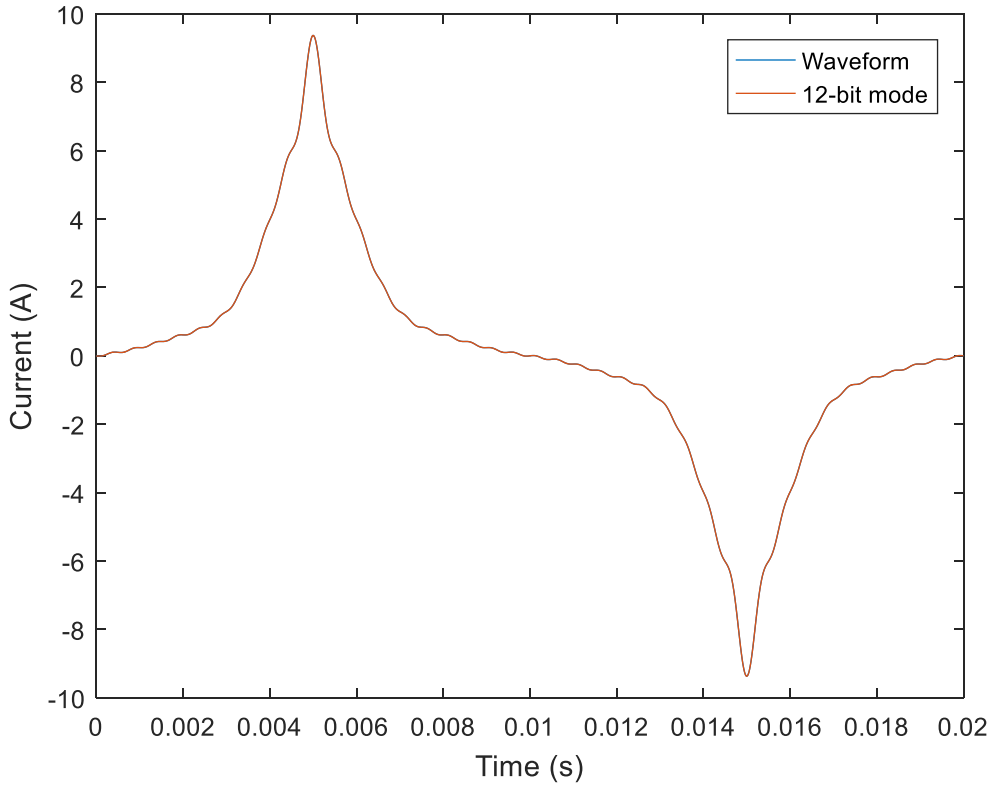

Figure 3: Example IEC waveform with a 50Hz fundamental.

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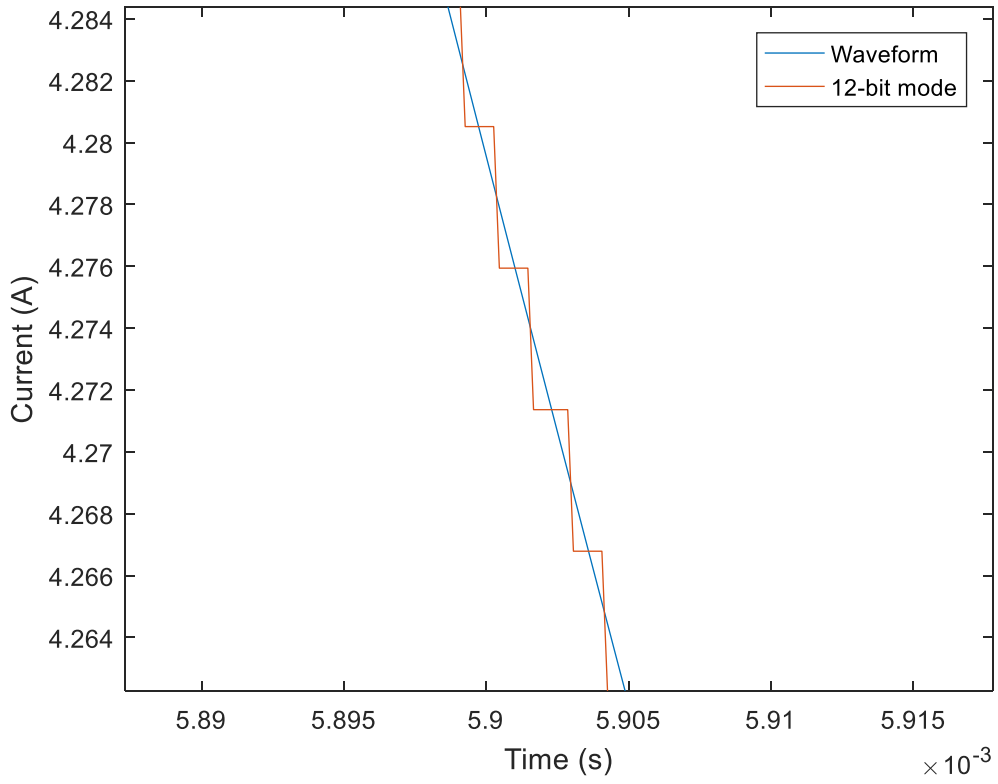

Figure 4: Example IEC waveform - high zoom to show quantisation.

The primary features of the wave form.

Table 3: IEC waveform parameters	
Parameter	**Value**
Fundamental Frequency	50 Hz
Peak	9.3686 A
RMS	3.1401 A
Crest Factor	3

3.5 ANALYSING THE WAVEFORM

To analyse the waveform the DFT was calculated using the equation:

$$Magnitude(f) = \left| \sum_{n=1}^{N} v[n] \cdot e^{-j2\pi f t[n]} \right| \cdot \frac{2}{N}$$

This function can then be used to extract the 39 harmonics in the waveform for both the original waveform and the 12 bit quantised waveform, as shown in Figure 5 plot A.

It is clear from the stem plot that the error terms are very small, so the error has been calculated as a percentage to help visualise the relative magnitudes.

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Figure 5 plot B shows the error term of the 12-bit harmonics, in relation to the spec of the PPA55 at that point for a 10Amp range, and the reproducibility tolerance in the IEC standard $(1\% + 10mA)$.

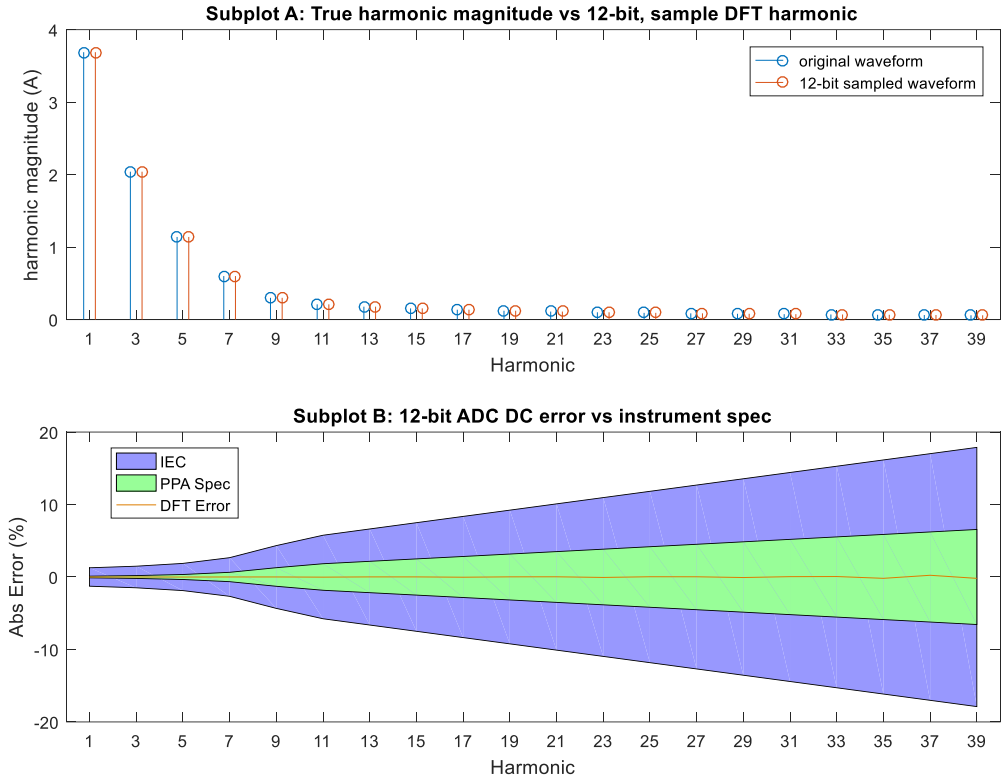

Figure 5:Subplot A: harmonic decomposition of IEC waveform; Subplot B: Magnitude of harmonic error

3.6 RMS OF COMPLEX WAVEFORM

Continuing from Section 3, the question of how the RMS error would compare for a more complex (non-sinusoidal) AC waveform.

Repeating the same methodology but using the IEC waveform, Figure 6 shows the RMS error. The envelope of the waveform is slightly different, which is expected since there are multiple components in the waveforms, but the limits to the error are nominally the same. It is also clear that beyond ~10 bits, any error becomes an immaterial component of overall system specification.

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Figure 6

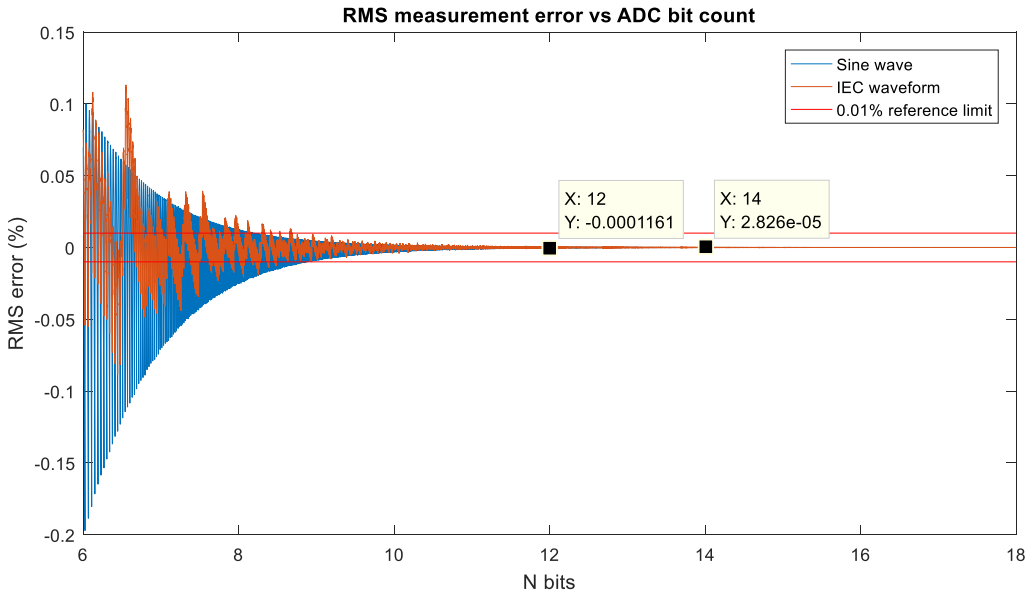

Figure 6: Error is sampled RMS measurement for the IEC and sine waveforms with varying ADC sizes

4 CONCLUSION

The examples in this document illustrate that the contribution of error associated with quantization in an ADC above 10 bits is a small proportion of the overall system performance, and therefore simply increasing bits with the aim of increasing overall system accuracy becomes futile.

Modern power analyzers utilise hardware ranging and analogue signal conditioning to optimise performance of ADCs and can provide a greater dynamic range than a fixed range system, with a high bit count.

Designing an accurate measurement system requires the balance and consideration of multiple components and each stage of signal conditioning; determining the accuracy of a measurement system is never as straightforward as identifying the number of bits used in the ADC.

Taking any singular performance characteristic cannot be used in isolation to calculate overall performance of any measurement instrument. Furthermore, while theoretical accuracy computation as illustrated in this document is helpful to determine the point at which specific aspects of a design have been optimised, the overall performance must always be validated through direct and traceable calibration.

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